**ICS233 Lab Project-T211: Test Cases**

1. **Initializing Registers (Testing I-Type ALU):**

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| **Instruction** | **Hexadecimal** | **Expected Result** |
| **ORI R1, R0, 3** | **3023** | **R1 = 3** |
| **ORI R7, R0, 7** | **30E7** | **R7 = 7** |
| **CANDI R3, R1, 7** | **2967** | **R3 = 4** |
| **ANDI R2, R1, 5** | **2145** | **R2 = 1** |
| **XORI R4, R1, 6** | **3986** | **R4 = 5** |
| **ADDI R6, R5, 0x0d** | **45CD** | **R6 = 0x000d** |
| **NADDI R4, R3, 10** | **4B8A** | **R4 = 6** |
| **SEQI R5 R4 0x1f** | **54AF** | **R5 = 0** |
| **SLTI R3, R6, 0x0E** | **5E6E** | **R3 = 1** |

1. **Testing R-Type ALU, Branches, SW, LW and J Instructions**

**(NO RAW hazards – NO Forwarding)**

|  |  |  |
| --- | --- | --- |
| **Instruction** | **Hexadecimal** | **Expected Result** |
| **AND R4, R2, R3** | **0270** | **R4 = 1** |
| **CAND R7, R7, R1** | **073D** | **R7 = 0** |
| **OR R3, R1, R4** | **018E** | **R3 = 3** |
| **XOR R3 R1 R2** | **014F** | **R3 = 2** |
| **ADD R3, R2, R1** | **094C** | **R3= 4** |
| **NADD R5, R1, R3** | **0975** | **R5 = 1** |
| **SEQ R6, R4, R3** | **0C7A** | **R6 = 0** |
| **SLT R5, R2, R3** | **0A77** | **R5 = 1** |
|  |  |  |
| **SLL R4, R3, 2** | **6382** | **R4 = 16** |
| **SRL R5, R3, 2** | **6BA2** | **R5 = 1** |
| **SRA R6, R3, 2** | **73C2** | **R6 = 1** |
| **ROR R7, R3, 2** | **7BE2** | **R7 = 1** |
|  |  |  |
| **BEQ R2, R5, 4** | **8544** | **Branch is taken #Skipp 3 instructions** |
| **NOP** | **0000** | **No operation** |
| **NOP** | **0000** | **No operation** |
| **NOP** | **0000** | **No operation** |
| **NOP** | **0000** | **No operation** |
| **BNE R2, R5, 4** | **8D44** | **Branch is not taken** |
| **BLT R5, R2, 6** | **92A6** | **Branch is not taken** |
| **BGE R3, R7, 2** | **9BE2** | **Branch is taken #Skipp 1 instruction** |
| **NOP** | **0000** | **NOP** |
| **NOP** | **0000** | **NOP** |
|  |  |  |
| **SW R4, 0(R5)** | **AD80** | **Mem[R5] = R4 = 0x10** |
| **SW R3, 2(R0)** | **A862** | **Mem[2] = R3 = 0x4** |
| **LW R1, 0(R5)** | **A520** | **R1 = Mem[R5] = 0x10** |
|  |  |  |
| **J 3** | **E003** | **#Skipp 2 instructions** |
| **NOP** | **0000** | **NOP** |
| **NOP** | **0000** | **NOP** |
| **JAL 2** | **E802** | **#Skipp 1 instruction** |
| **NOP** | **0000** | **NOP** |
| **JALR R2, R1** | **D940** | **R2 = 0x28, PC = 0x10** |
| **#NOTE: the bellow cannot be reach, add it manually** | | |
| **ADDI R1, R0, 1** | **4021** | **R1 = 0x21 = 33** |
| **IMM 1** | **F001** |

1. **Testing RAW hazards and Forwarding**

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| **Instruction** | **Hexadecimal** | **Expected Result** |
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1. **Testing Load delay, stalling pipelining, and forwarding after LW**

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| **Instruction** | **Hexadecimal** | **Expected Result** |
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